7. OPERATION OF THE MODULES

7-1. TX Module

See (1A2) Circuit Diagram of TX Module: 33-106054 and Fig. 7-1 Basic Block Diagram of TX Module.

7-1-1. General

The TX module consists of a low-frequency signal circuit, and FM modulator, a phase-locked loop using a high-output voltage-controlled oscillator (VCO), and a power circuit.

Voice signals (300 Hz to 3KHz), tone signals (2400 Hz) and digital signals (300 bps 4 phase, DPSK) input from the MCC are processed by the low-frequency signal circuit and fed to the FM modulator. The phase- locked loop (PLL) mixes the frequency-modulated signal from the modulator with a multi-channel local signal from the frequency synthesizer. Frequency multiplication, power amplification, and filtering through a bandpass filter in the PLL then produce a high-output multi-channel modulated signal in the transmit frequency band at the output terminal. This signal is sent to the POW AMP module.

7-1-2. Principles of Operation

(1) Low-frequency signal circuit

The low-frequency signal circuit consists of filter circuits and an amplifier/limiter circuit. The voice, tone, and digital signals from the MCC are led to pin 10 of connector Z203. Band and amplitude limitaiton are performed by a 300 Hz high-pass filter (HPF) in IC2 (TH-032), a 6 dB/octave pre-emphasis circuit formed by C2 and R2, an amplifier/limiter circuit in IC3 (CA3130E), and a 3 KHz low-pass filter (LPF) in IC4 (TH-031), after which the signal is sent to the FM modulator built around IC1 (TH-033).

(2) FM modulator

The FM modulator functions by means of a voltage-controlled crystal oscillator (VCXO) composed of a 14.925 MHz crystal oscillator (Y1), a variable capacitance element (X1), and a Colpitts oscillation circuit (IC1: TH-033). The oscillation frequency of the VCXO is controlled by the voltage applied to the variable capacitance element connected to the crystal oscillator, so frequency modulation is achieved by superimposing the processed signals from the low-frequency signal circuit on this applied voltage. The frequency deviation of the modulated 14.925 MHz signal output by the FM modulator is quadrupled by the phase-locked loop, as described later, so the standard frequency deviation here is set at ±3 KHz/4 = ±0.75 KHz.

(3) Phase-locked loop (PLL)

See the basic block diagram of TX module in Fig. 7-1. The PLL circuit is a closed loop consisting of a phase detector (PD), low-pass filter (LPF), voltage-controlled oscillator (VCO), frequency mixer (MIX), bandpass filter (BPF), and 1/4 fixed frequency divider (DIV). These blocks are indicated on the circuit diagram of the TX module (33-106054) as follows:

PD: IC1 of A1 PD sub-module

LPF: TR2 and TR6, and peripheral circuits thereof

VCO: TR4, X3, and L2, and peripheral circuits thereof

MIX: TR8

BPF: L9 and TR7, and peripheral circuits thereof

DIV: IC2 of AL PD sub-module

* The PD sub-module means the PD and the DIV.

The phase detector compares the phase of the modulated 14.925 MHz signal output from the FM modulator with the phase of the frequency output from the divider and generates a DC voltage proportional to the phase difference. Noise and leakage signals riding on this DC voltage output are attenuated by the LPF. The VCO generates a frequency F_T in the range from 450.350 to 452.325 MHz, proportional to the voltage output of the LPF. The frequency output F_T from the VCO is branched: one branch is buffered by the TR_5 (2SC1426) circuit and becomes the output

of the TX module; the other branch is buffered by the TR9 (2SC2026) circuit and fed to the mixer (TR8).

The mixer also receives a multi-channel local frequency F_L from the synthesizer mudule via TR10 (2SC2026). It mixes the frequency of F_L with that of F_T from the VCO. The bandpass filter, which is formed by TR7 (2SC460) tuning amplifier and L9, extracts the differential frequency 59.7 MHz resulting from the frequency mixing, eleiminate other unwanted frequencies, and feeds the 59.7 MHz to the divider. The divider divides the 59.7 MHz frequency by 4 to produce a 14.925 MHz output, which is returned to the phase detector.

The phase-locked loop thus automatically controls the VCO frequency so that the 14.925 MHz modulated frequency input to the phase detector matches the frequency of the divider output signal at all times. The frequency function when the PLL is on lock is:

$F_T = F_L + (N \times F_M)$

where F_T: VCO oscillation frequency (450.350 - 452.325 MHz)

F_L: Multi-channel local Frequency (390.650 - 392.625 MHz)

F_M: Center frequency of modulated frequency (14.925 MHz)

N : Divider factor (4)

If the PLL is locked on channel 1, then:

450.350 MHz = 390.650 MHz + (4 x 14.925 MHz)

F_T (CH1) F_L N F_M

In this locked state, if F_M is modulated to produce a frequency shift, F_T shifts by 4 times the same amount. If F_L is changed to switch channels, F_T tracks the change. This operation provides a maximum of 80 modulated frequencies (80 channels) in the 450.350 to 452.325 MHz range, spaced at intervals of 25 KHz.

Although the oscillation frequency of the VCO is controlled by the output voltage of the low-pass filter, its oscillation output level is independent. The gain of the output amplifier can therefore be held down by maintaining a high VCO output level and such low gain reduces noise in the output signal. The high power level of the VCO output is approximately 100mW.

As described above, the VCO in the phase-locked loop is controlled indirectly by the output voltage of the phase detector via the low-pass filter. As a safety measure in case the PLL loses its lock, an alarm circuit (X1, X2, and TR3 in the PD sub-module) is added to the output circuit of the phase detector. The alarm circuit detects also no presence of phase detector input signal as no lock state of PLL. The alarm signal from this circuit is sent to the power amplifier module through pin 4 of connector Z203 and stop the RF power amplifier to prevent transmission of an uncontrolled signal.

(4) Power circuit

The power circuit consists of voltage regulator circuits that

convert a +13.2V input to +9.0V, +8.0V, +7.8V, and +5.0V outputs, and a switch circuit that switches the regulated output voltages on and off according to the TX key signal sent from the MCC.

The +13.2V fed from the PS module is input to the regulator chip IC5 (μPC14308H or μPC7808H) via pin 2 of connector Z203. The regulated +8.0V output from the IC5 is supplied to the low-frequency signal circuit (IC2, IC3, and IC4), the FM modulator (IC1), and TR3 in the alarm detection circuit.

The +9.0V output is regulated by IC6 (TH-035 or TH-077) and TR11 (2SB744) and supplied to TR4 in the VCO and to the buffer circuits (TR5 and TR9).

The +7.8V output is regulated by IC6 and supplied to TR7 in the bandpass filter, TR8 in the mixer, and TR10 in the buffer circuit.

The +5.0V output is regulated by IC6 and supplied to the phase detector (IC1) in the PD sub-module and the divider (IC2).

The TX key signal from the MCC is input to IC6 via pin 3 of connector Z203. It controls the +9.0V, +7.8V, and +5.0V outputs, turning them off during non-transmission (in the ready-to-receive state) to reduce current drain.

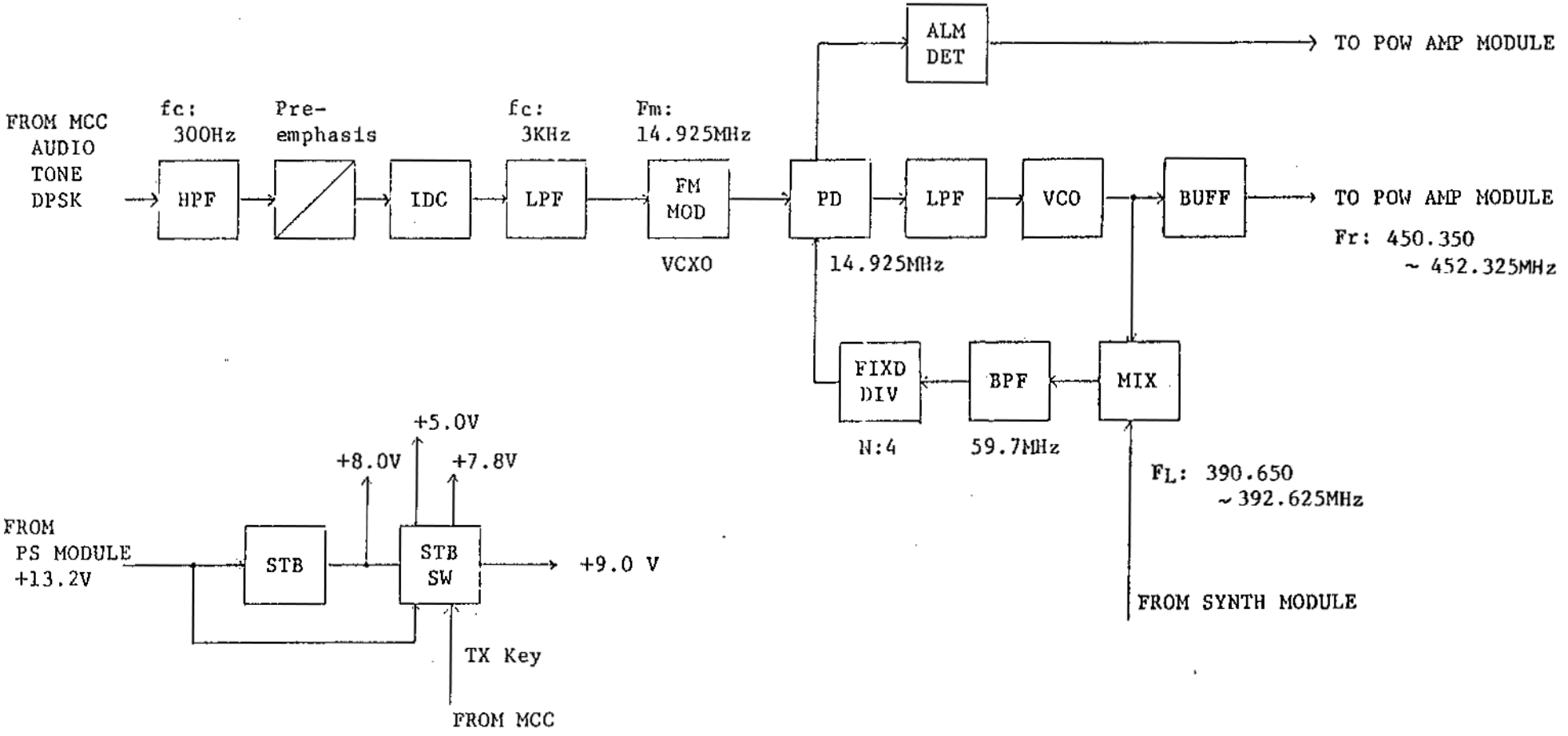

Figure 7-1 BASIC BLOCK DIAGRAM OF TX MODULE

7-2. POWER AMP Module

See (1A3) Circuit Diagram of POWER AMP Module: 33-106055.

7-2-1. General

The POW AMP module amplifies the power of the 450.350 to 452.325 MHz frequency-modulated signal from the TX module to a designated output level. It consists of a RF power amplifier module, in which three transistor stages are integrated, and its control circuits. The functions of the control circuits include automatic power control (APC) to maintain stable transmitter output, power reduction to restrict the transmitter output level, switching the transmitter output on and off, monitoring the transmitter output, and monitoring the operating temperature of the RF power amplifier module.

7-2-2. Principles of Operation

(1) RF Power Amplifier Module

In the RF power amplifier module, IC1 (TG-3Q0-0049) raises the level of the +22 dBm signal received from the TX module by about 21 dB to deliver over 20W of output power. Each transistor in three transistor stages has a grounded-emitter. The degree of amplification can be controlled or the amplification function stopped altogether by controlling the voltage at pin 5, which is connected to the collector of the first-stage transistor. The

impedance of the output at pin (1) of IC1 is matched by a micro-stripline formed on the triazine printed circuit board (dielectric constant 4.2) to produce the output signal.

(2) Control circuits

(a) Automatic power control (APC)

The APC adopts a negative-feedback control system and regulates the output of the RF power amplifier module by depressing variations in the output power of IC1 caused by variations the supply voltage or ambient temperature. It has a closed-loop configuration consisting of X1 (1SS16), IC2:1/2 (μPC251), TR2 (2SC460), TR1 (2SB707), and IC1. Part of the output signal from IC1 is rectified by X1 and input to the voltage comparator in IC2:1/2. Z1 is a posistor used for temperature compensation and monitoring temperature rise in the rectifying circuit of X1.

IC2:1/2 compares the rectified voltage from X1 with a reference voltage generated by R15, RV1, and R14 and amplified the difference voltage. This amplified difference voltage is further amplified by TR2 and TR1, then fed to pin 5 of IC1 to control its RF power amplification function. Since the APC closed-loop operates to match the rectified voltage from X1 to the reference voltage in IC2:1/2, in output at normal power (when the output power reduction function is not used), the output power can be set freely by adjusting RV1.

(b) Reduction of transmitter output power

The transmitter output power reduction function reduces the transmitter output power by about 10 dB from its normal 15W on command from the MCC. (The reduced transmitter output powers are adjusted to approximately 5W and 2W.) The command i.e. PWR CONT signal from the MCC reaches the TR5 and TR7 (2SC460) switch circuit through pin 3 of connector Z204. When TR5 is turned on by the MCC command, the foresaid reference voltage of the APC (the voltage at pin 3 of IC2:1/2) is lowered forcedly by RV2. By this, medium power ("M" power) can be gained. When TR5 and TR7 are turned on by the MCC command, the foresaid reference voltage of the APC is lowered forcedly by RV3. (Note: Since RV2 is already set to "M" power, do not turn it.) By this, lower power ("L" power) can be gained. The APC closed-loop tracks this operation, thus lowering the output power of IC1 in the RF power amplifier module. The APC continues to operate during low-power transmission, and "M" power level can be set by adjusting RV2 and "L" power level can be set by adjusting RV3.

(c) Power monitor

The power monitor monitors the presence of the transmitter output signal and sends detection information to the PS module and the MCC. The power monitor detection signal is obtained by amplifying the rectified output voltage of X1 by IC2:1/2 and converting it to a logic-level signal by TR4 (2SC460). It is supplied to pin 2 of connector Z204.

(d) Transmitter output on/off control

Normally the transmitter output is turned on and off by commands from the MCC, but it can also be controlled by the TX-ALARM signal sent from the TX module and by thermal information from the thermal sensor incorporated in the POW AMP module. The TX-ALARM signal is issued when the PLL loses its lock in the TX module. When the TX-ALARM signal is detected by the POW AMP module, transmitter output is shut down and transmitter-off information is sent to the PS module and the MCC.

The thermal sensor monitors the surrounding temperature of the RF power amplifier module. The detection threshold is about 60°C; when this temperature is exceeded, transmitter output is reduced. The RF power amplifier module normally operates at a fairly high temperature.

The power on/off signal (TX-key signal) from the MCC is input to TR3 (2SC460) from pin 4 of connector Z204 via X2 (1S953). The TX-ALARM signal from the TX module is input to TR3 from pin 5 of connector Z204 via TR6 (2SC460) and X3 (1S953). TR3 is a switch circuit that turns TR2 and TR1 in the APC on and off. If it receives even one of the above two signals, it applies an OFF voltage to pin 5 of IC1 to kill the power amplification function.

(3) Power circuit

Since the POW AMP module consumes a large amount of current during

transmission, it receives +13.2V power suppy directly from the PS module instead of via the printed circuit board and connector. The control circuits operate on a regulated +8.0V power supply regulated by IC3 (NJM78L08A) from this +13.2V. IC1 operates directly on the +13.2V supply.

7-3. TX BEF (TX Band-Eliminate Filter)

See (1A4) Circuit Diagram of TX BEF: 34-103764.

The TX BEF is band-eliminate filter that reduces local receiver-band noise (F_R: 460.350 to 462.325 MHz) in the output signal of the POW AMP module, to prevent receiver sensitivity degradation during transmission. The filter consists of three high-Q dielectric resonators and $\lambda/4$ connecting circuits.

7-4. Circulator

See (1A5) Circuit Diagram of Circulator: 34-103765.

The circulator module, which acts as the antenna duplexer, consists of the circulator itself, a matching circuit, and a low-pass filter to reject harmonic frequencies. The circulator is built to be only 0.5 dB or less in insertion loss of the transmitter signal so that it can withstand continuous duty on 15W transmission.

7-5. RX BPF (RX Bandpass Filter)

See (1A6) Circuit Diagram of RX BPF: 34-103766.

The RX bandpass filter passes the receive band (460.350 to 462.325 MHz) and attenuates all other frequency bands. It consists of six high-Q dielectric resonators and their connecting circuits. Since it requires a particularly strong attenuation characteristic in the local transmit band of the transceiver, three of the six resonator stages act as band-eliminate filters. The pass-through loss of the RX BPF is 3 dB or less.

7-6. RX Module

See (1A7) Circuit Diagram of RX Module: 33-106056

7-6-1. General

The RX module consists of a high-frequency amplifier circuit that selects and amplifies the receive-band signals input from the RX band-pass filter, an intermediate-frequency converter/demodulator circuit that extracts and demodulates the desired signal from the receive-band signals, a low-frequency signal circuit that selects and amplifies the demodulate output, and a power circuit. Tuning to the

desired receiver signal is made by a frequency synthesizer controlled by the MCC. As output from the RX module, the MCC receives the demodulated voice, tone, and digital signals and the squelch and carrier detect signals.

7-6-2. Principles of Operation

(1) High-frequency amplifier circuit

After the signal input from the RX BPF is amplified by TR1 (2SC3358) and filtered by a bandpass filter (BPF3) to reject unwanted frequencies outside the receive-band, it is injected to the first mixer TR2 (2SC3358). The bandpass filter (BPF3), which uses two LC tuning circuits printed on a mica substrate, both attenuates out-of-band spurious signals and matches impedance with the first mixer.

(2) Intermediate-frequency converter/demodulator circuit

The high-frequency received signal (F_R: 460.350 to 462.325 MHz) and the first local signal (F_L: 390.650 to 392.625 MHz) input from the frequency synthesizer via the buffer circuit TR5 (2SC2026) are injected to the base of TR2 (2SC3358), the first mixer, which derives and outputs the first intermediate frequency of 69.700 MHz. THis output signal is passed through a 69.700 MHz two-element monolithic crystal filter (MCF), BPF1 (1/2), and BPF1 (2/2) to reject spurious signals and amplified by TR3 (2SC2026), then fed to the PIN 16 of IC1.

This signal is input to pin 16 of intergrated circuit (IC1). IC1 (IR3N37) includes second mixer, second local oscillator, limiting amplifier, quadrature discriminator and carrier signal output terminal. The frequency of second local signal is made to 69.245 MHz by connecting 3rd-overtone crystal oscillator Y1 to pin 1 of IC1.

The input signal of pin 16 of IC1 and second local signal are mixed by mixer of IC1, and 455 KHz is extracted. This output signal passes through ceramic filter (BPF3) with center frequency of 455 KHz connected between pin 3 and 4 terminals of IC1 and the unnecessary wave of signal is eliminated. FM modulated signal of 455 KHz is amplified and limited at IC1, and demodulated at quadrature discriminator, it is output to pin 9 of IC1 as low frequency signal.

(3) Carrier-detect circuits

The squelch and carrier-detect functions are carried out by an RF input field strength detection method with excellent dynamic characteristics and low failure rate. The detectors are IC4 (TH-105) and IC5 (TH-030), each of which consists of an amplifier and rectifier circuit. They monitor the 455 KHz second intermediate-frequency signal branched from the output pin 4 of IC1. This signal is proportional to the RF input level variation.

IC4 are high-level carrier detector (CDH) and a medium-level carrier detector (CDM) which detect whether the input field strength at the antenna terminal exceed 20 dBμ or not and 15.5 dBμ or not. The detection signal is sent to the MCC via pin 8 and 6 of connector Z205. IC5, the low-level carrier detector (CDL), detects whether the input field strength at the antenna terminal exceeds 0 dBμ or not. This detection signal is sent to the MCC and the autonomous circuit in the PS module via pin 9 of connector Z205.

(4) Low-frequency signal circuit

The low-frequency signal demodulated by IC1 is amplified by TR4 (2SC460). IC2 (F205A) is a 300 Hz to 3 KHz active band-pass filter. After being thus limited, the low-frequency signal passes through a -6 dB/octave de-emphasis circuit composed of R25 and C30, then is amplified by IC10:1/2 (μPC251). The output level of this low-frequency signal is adjusted to be -10 dBm in the standard modulation condition (frequency deviation ±3 KHz, modulation frequency 1 KHz) when terminated by a 600 Ω load resistor. The amplified low-frequency signal is supplied to the MCC via pin 5 of connector Z205.

(5) Power circuit

The +13.2V input from the PS Module is supplied through pin 2 of connector Z205 to the regulator IC11 (NJM78L08A or μPC7808H). The +8.0V output voltage from IC11 powers the entire RX module.

7-7. SYNTH Module

See (1A8) Circuit Diagram of Synthesizer Module: 33-106057 and Simple Block Diagram of Synthesizer Module Figure 7-2.

7-7-1. General

The Synthesizer module generates the local signals supplied to the TX and RX modules. Its output frequency is selected by command from the MCC. It operates as a digital frequency synthesizer, using direct oscillation and direct frequency division in a phase-locked loop (PLL) principle. It consists of a voltage-controlled oscillator (VCO) that oscillates directly at the local frequency, a PLL circuit that makes direct variable division of this frequency and then controls the phase of the devided frequency by means of a reference oscillator, and a power cirucit.

The VCO circuit is housed in an aluminum die-cast case so that vibration and shocks will not generate noise. A micro-stripline formed on a low-loss dielectiric substrate acts as the oscillation tuning coil of the VCO.

The direct variable divider in the phase-locked loop operates by the pulse-swallow principle, and is configured with a low-power bipolar prescaler and CMOS programmable counter. The reference signal for the phase-locked loop is obtained by dividing the frequency of a temperature-compensated crystal oscillator (TCXO).

7-7-2. Principles of Operation

(1) PLL circuit

Figure 7-2 gives a simple block diagram of the synthesizer module. The notations in Fig. 7-2 correspond to those in (1A8) Circuit Diagram of Synthesizer Module: 33-106057 as follows.

Circuit/symbol in Fig. 7-2	Circuit/symbol in 33-106057
TCXO	OSC1
DIV, PD, Programmable counter	IC1
Prescaler	IC2
LPF	TR2, TR3, TR4, TR5
ALM-DET	TR1, X1, X2
BUFF1	TR7
BPF	T1, T2 and Peripheral circuits thereof
BUFF2	TR8
BUFF3	TR6
BUFF4	TR9
STB1	IC3
STB2	TR10, TR11

The PLL circuit consists of a TCXO, phase detector, low-pass filter (LPF), volgate-controlled oscillator (VCO), buffer amplifier (BUFF1), bandpass filter (BPF), BUFF2, BUFF3, a prescaler, and a programmable counter, connected in a closed loop except TCXO.

The TCXO, a crystal oscillator with a thermistor element for temperature compensation, oscillates at a frequency F_R of 12.800 MHz. Its frequency output is divided by a factor N_R of 512 by the divider (DIV) to produce a frequency f_r of 25.000 KHz which is sent to the phase detector (PD) as the reference frequency of the phase-locked loop.

The phase detector compares the phase of the reference signal f_r with that of the programmable counter and puts out a DC voltage proportional to the phase difference. The low-pass filter attenuates noise and reference-signal leakage superimposed on the phase-detector output. The voltage output of the low-pass filter is fed to the VCO, which oscillates at a frequency proportional to the voltage. The range of the VCO oscillation frequency F_L is 390.650 to 392.625 MHz. The VCO output signal is branched inside the case, with one part supplied directly as the local signal of the TX module.

The other branch of the signal is passed through BUFF1, BPF, and BUFF2 for high-frequency amplification and bandpass filtering, then supplied through BUFF4 as the local signal of the RX Module and through BUFF3 as the prescaler input. The prescaler and the programmable counter combine to divide the input signal by a factor of 15,626 to 15,705; the divided signal is then fed to the phase detector. The precise factor by which the prescaler and programmable counter divide the signal is determined by the data, strobe, and clock signals received from the MCC through pins 3,

4, and 5 of connector Z206. The division factor combined by the prescaler and programmable counter according to these command signals is shown in Table 7-1.

The PLL circuit operates as a negative feedback system that automatically controls the oscillation frequency of the VCO so that the frequency of the output signal from the programmable counter always matches with that of the reference signal f_r input to the phase detector. When the PLL is on lock, the various frequencies in it are related as follows:

$$F_L = f_r \times (N_V \times N_P) \qquad f_r = \frac{1}{N_R} \times F_R$$

where F_L : VCO oscillation frequency (390.650-392.625 MHz)

f_r : PLL reference frequency (25 KHz)

F_R : TCXO oscillation frequency (12.800 MHz)

N_R : Division factor of programmable counter

N_P : Division factor of prescaler

$(N_V \times N_P)$: Combined division factor of programmable counter and prescaler (15,626-15,705)

If the PLL is locked on channel 1, then:

390.650 MHz = 25 KHz x 15,626

(F_L: CH1) (f_r) ($N_V \times N_P$)

If the MCC commands the prescaler and programmable counter to divide by a factor of 15,627, which corresponds to channel 2,

the VCO will be controlled to oscillate at a frequency F_L of 390.675 MHz. As its output frequency is moved through the range from 390.650 to 392.625 MHz in this way, it provides local signals for 80 transmitter and receiver channels with a channel spacing of 25 KHz. The stability of the frequencies for all channels is controlled by the TCXO.

As described above, the VCO is controlled indirectly by the PLL circuit through the phase detector output voltage. An alarm circuit, which is same as the alarm circuit incorporated in the TX module, is also provided to the SYNTH module in case the PLL gets out of lock. The alarm signal from this circuit is sent to the MCC through pin 10 of connector Z206. On receiving the alarm signal, the MCC shuts down the whole radio section.

(2) Channel switching

The output frequency of the synthesizer module is set by a channel switching command from the MCC. The command is given as a 17-bit binary input code corresponding to the radio channel number. Table 7-1 shows the transmit frequency F_T, receive frequency F_R, synthesizer output frequency F_L, combined division factor N (= N_V x N_P), and the program input value from the MCC for each radio channel number. A block diagram of the prescaler and programmable counter is shown in Fig. 7-3.

The data signal (which gives the input code specifying the radio

channel) from the MCC is clocked into a shift resister by the clock signal. The information in the shift register is moved to another resister by the strobe signal from the MCC, from which it controls the division module of the A counter and N counter. The A counter output controls the division factor of the prescaler, setting it to either 64 or 65. The N counter controls the A counter and produces the properly divided output signal.

Figure 7-4 is a timing chart of the data signal, clock signal, and strobe signal sent from the MCC. The MCC sends these channel-specifying signals only when switching channels; it stops sending them after switching has been accomplished.

(3) Voltage-controlled oscillator (VCO)

See (1A8A1) Circuit Diagram of VCO: 34-103769.

The VCO consists of a common-base Colpitts oscillation circuit and a buffer amplifier circuit, and is mounted on a low-loss dielectric substrate. The oscillation tunig coil of the VCO is a $\lambda/2$ micro-stripline formed on the substrate, and the tuning capacitor circuit of the VCO includes a varactor diode that adjusts the oscillation frequency in response to a control voltage sent from the phase detector through the low-pass filter.

The Colpitts oscillation circuit formed by the varactor diode X1 and transistor TR1 oscillates at frequencies from 390.650 to

392.625 MHz. Its frequency output is amplified by the TR2 buffer amplifier, then branched. One branch is further buffered by TR3 and TR4 and fed directly to the TX module as the local signal of the transmitter. The other branch is buffered by TR5 and used as both the feedback signal to the PLL and the local signal of the receiver. The various buffer amplifiers in the VCO are provided to prevent unwanted signals and noise from the outside from entering the oscillation circuit.

Notes:

The inside of the VCO is precisely adjusted before shipment and should not be tampered with. Opening the cover will only let in dust.

Handle the VCO with care to avoid strong vibration or shock. (Don't drop it.)

(4) Power circuit

The synthesizer module operates on +8.0V and +5.0V Power. The +13.2V input from the PS module is led through pin 2 of connector Z206 to IC3, which delivers a regulated +8.0V output. The +5.0V supply is regulated from the +8.0V by IC4. The +8.0V supply powers the buffer circuits, low-pass filter, and VCO in the phase-locked loop. The +5.0V supply powers the TCXO, IC1, IC2, and the alarm circuit.

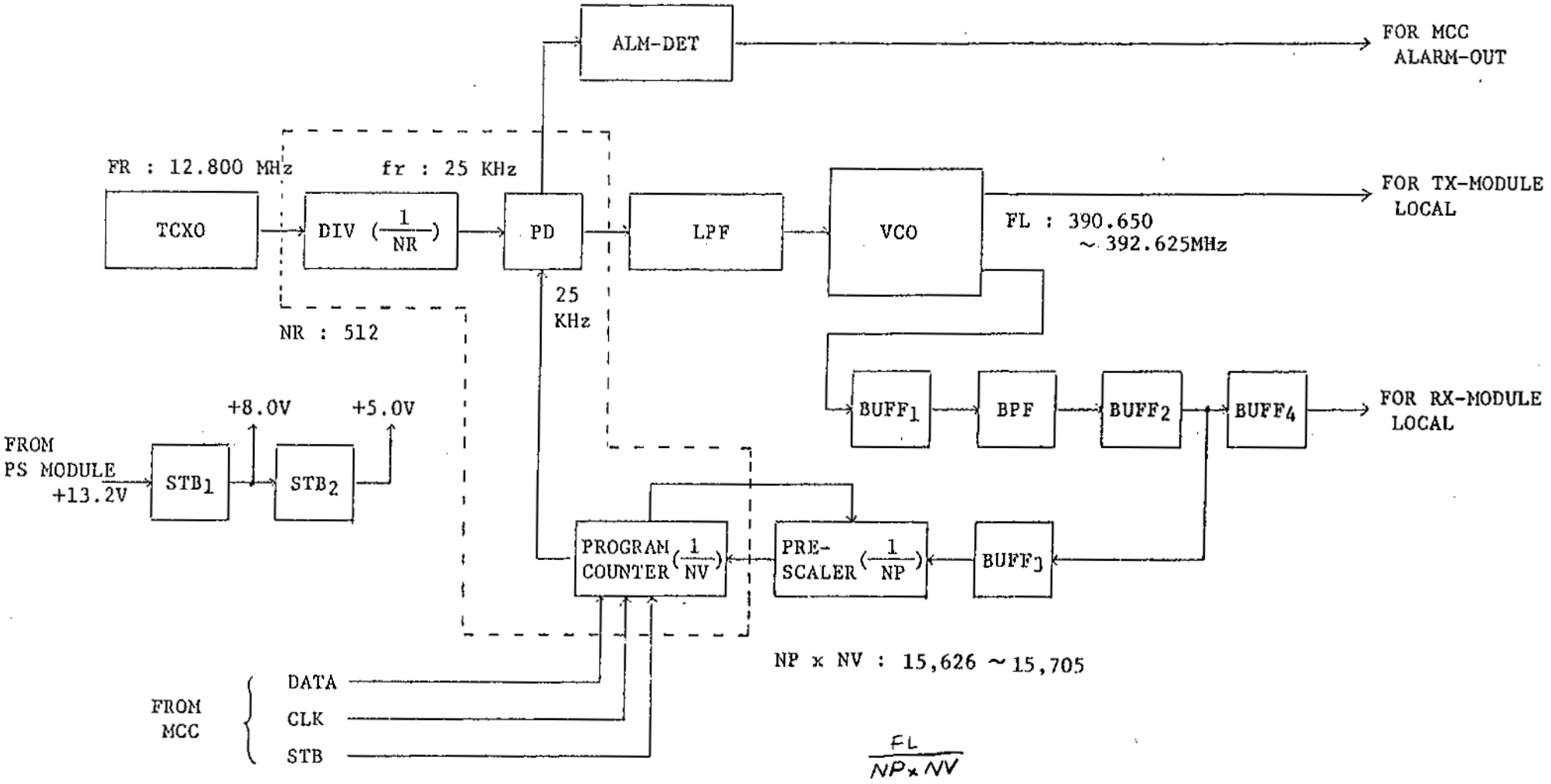

Figure 7-2 SIMPLE BLOCK DIAGRAM OF SYNTHESIZER MODULE

Table 7-1

FREQUENCY - INPUT CODE

CH No.	F_T (MHz)	F_R (MHz)	F_L (MHz)	N(NvxNp)	*Program Input Value	
					N Counter Input	A Counter Input
1	450.350	460.350	390.650	15,626	244	10
2	450.375	460.375	390.675	15,627	244	11
3	450.400	460.400	390.700	15,628	244	12
4	450.425	460.425	390.725	15,629	244	13
5	450.450	460.450	390.750	15,630	244	14
6	450.475	460.475	390.775	15,631	244	15
7	450.500	460.500	390.800	15,632	244	16
8	450.525	460.525	390.825	15,633	244	19
9	450.550	460.550	390.850	15,634	244	18
10	450.575	460.575	390.875	15,635	244	19
11	450.600	460.600	390.900	15,636	244	20
12	450.625	460.625	390.925	15,637	244	21
13	450.650	460.650	390.950	15,638	244	22
14	450.675	460.675	390.975	15,639	244	23
15	450.700	460.700	391.000	15,640	244	24
16	450.725	460.725	391.025	15,641	244	25
17	450.750	460.750	391.050	15,642	244	26
18	450.775	460.775	391.075	15,643	244	27
19	450.800	460.800	391.100	15,644	244	28
20	450.825	460.825	391.125	15,645	244	29
21	450.850	460.850	391.150	15,646	244	30
22	450.875	460.875	391.175	15,647	244	31
23	450.900	460.900	391.200	15,648	244	32
24	450.925	460.925	391.225	15,649	244	33
25	450.950	460.950	391.250	15,650	244	34
26	450.975	460.975	391.275	15,651	244	35
27	451.000	461.000	391.300	15,652	244	36
28	451.025	461.025	391.325	15,653	244	37
29	451.050	461.050	391.350	15,654	244	38
30	451.075	461.075	391.375	15,655	244	39

* N Counter adopts 10-bit Binary Input Code.
A Counter adopts 7-bit Binary Input Code.

Table 7-1

FREQUENCY - INPUT CODE

CH No.	F_T (MHz)	F_R (MHz)	F_L (MHz)	N(NvxNp)	*Program Input Value	
					N Counter Input	A Counter Input
31	451.100	461.100	391.400	15,656	244	40
32	451.125	461.125	391.425	15,657	244	41
33	451.150	461.150	391.450	15,658	244	42
34	451.175	461.175	391.475	15,659	244	43
35	451.200	461.200	391.500	15,660	244	44
36	451.225	461.225	391.525	15,661	244	45
37	451.250	461.250	391.550	15,662	244	46
38	451.275	461.275	391.575	15,663	244	47
39	451.300	461.300	391.600	15,664	244	48
40	451.325	461.325	391.625	15,665	244	49
41	451.350	461.350	391.650	15,666	244	50
42	451.375	461.375	391.675	15,667	244	51
43	451.400	461.400	391.700	15,668	244	52
44	451.425	461.425	391.725	15,669	244	53
45	451.450	461.450	391.750	15,670	244	54
46	451.475	461.475	391,775	15,671	244	55
47	451.500	461.500	391.800	15,672	244	56
48	451.525	461.525	391.825	15,673	244	57
49	451.550	461.550	391.850	15,674	244	58
50	451.575	461.575	391.875	15,675	244	59
51	451.600	461.600	391.900	15,676	244	60
52	451.625	461.625	391.925	15,677	244	61
53	451.650	461.650	391.950	15,678	244	62
54	451.675	461.675	391.975	15,679	244	63
55	451.700	461.700	392.000	15,680	245	0
56	451.725	461.725	392.025	15,681	245	1
57	451.750	461.750	392.050	15,682	245	2
58	451.775	461.775	392.075	15,683	245	3
59	451.800	461.800	392.100	15,684	245	4
60	451.825	461.825	392.125	15,685	245	5

* N Counter adopts 10-bit Binary Input Code.
A Counter adopts 7-bit Binary Input Code.

Table 7-1

FREQUENCY - INPUT CODE

CH No.	F_T (MHz)	F_R (MHz)	F_L (MHz)	N(NvxNp)	*Program Input Value	
					N Counter Input	A Counter Input
61	451.850	461.850	392.150	15,686	245	6
62	451.875	461.875	392.175	15,687	245	7
63	451.900	461.900	392.200	15,688	245	8
64	451.925	461.925	392.225	15,689	245	9
65	451.950	461.950	392.250	15,690	245	10
66	451.975	461.975	392.275	15,691	245	11
67	452.000	462.000	392.300	15,692	245	12
68	452.025	462.025	392.325	15,693	245	13
69	452.050	462.050	392.350	15,694	245	14
70	452.075	462.075	392.375	15,695	245	15
71	452.100	462.100	392.400	15,696	245	16
72	452.125	462.125	392.425	15,697	245	17
73	452.150	462.150	392.450	15,698	245	18
74	452.175	462.175	392.475	15,699	245	19
75	452.200	462.200	392.500	15,700	245	20
76	452.225	462.225	392.525	15,701	245	21
77	452.250	462.250	392.550	15,702	245	22
78	452.275	462.275	392.575	15,703	245	23
79	452.300	462.300	392.600	15,704	245	24
80	452.325	462.325	392.625	15,705	245	25

* N Counter adopts 10-bit Binary Input Code.
A Counter adopts 7-bit Binary Input Code.

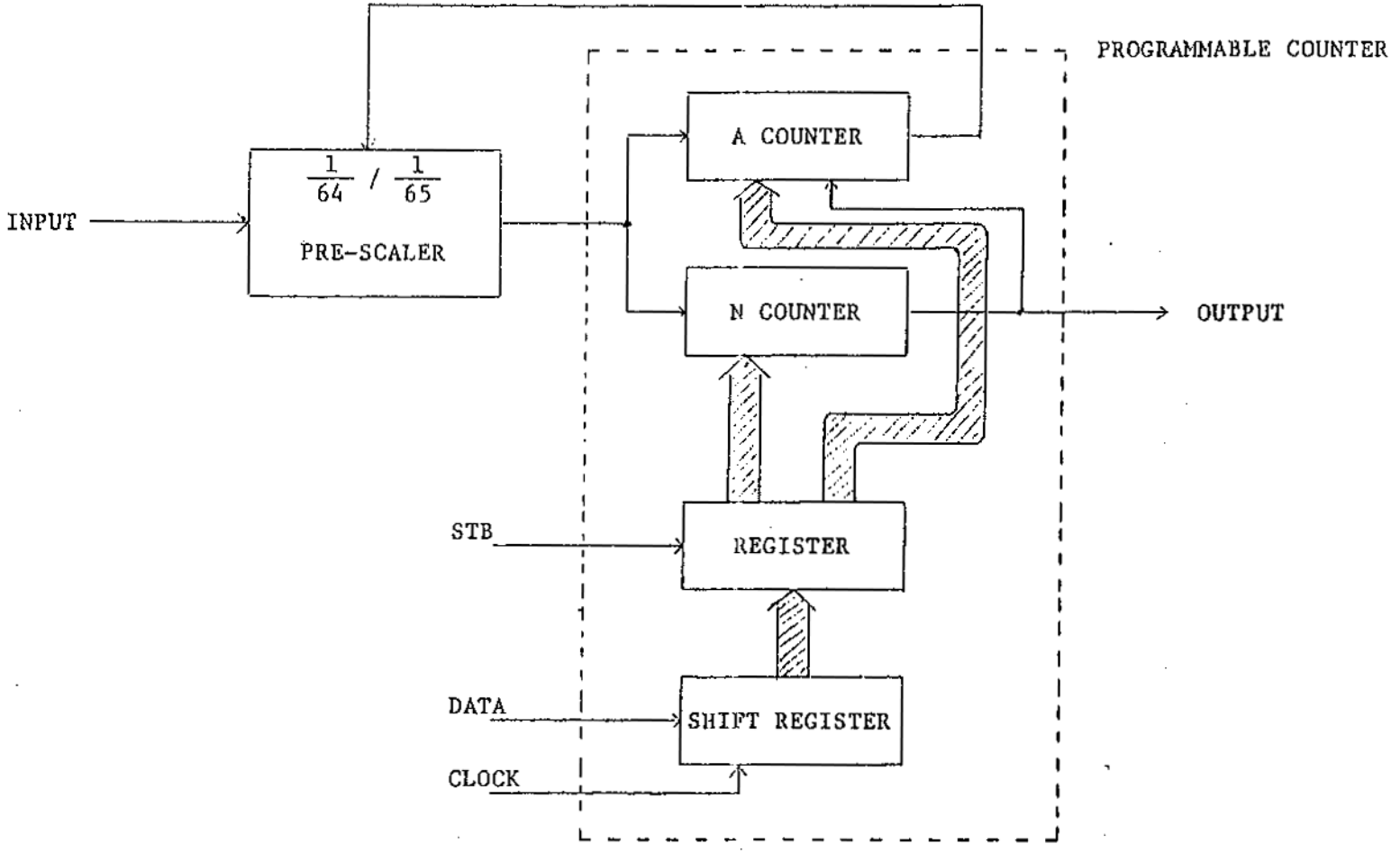

Figure 7-3 BLOCK DIAGRAM OF PRESCALER AND PROGRAMMABLE COUNTER

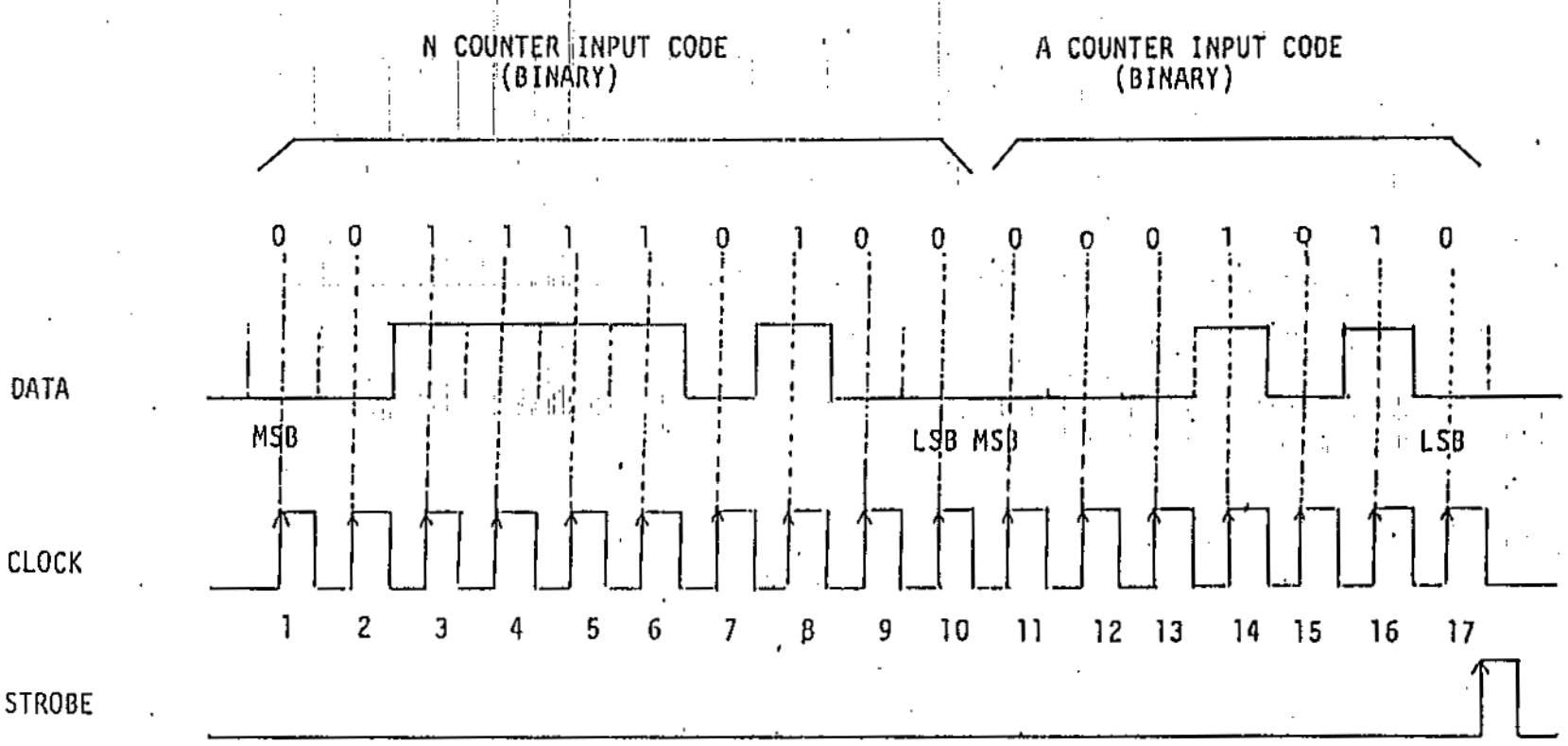

Fig 7-4 TIMING CHART OF DATA OF SIGNAL, CLOCK SIGNAL AND STROBE SIGNAL FROM MCC
(In case of designating 1 st channel.)

7-8. PS Module

See (1A9) Circuit Diagram of PS Module: 33-107412

7-8-1. General

The PS module smooths the +13.2V input from an external battery by removing noises and ripples and delivers power to the other radio section modules and the MCC. It consists of a main relay circuit to turn power on and off, a sub-relay circuit to drive the main relay, a smoothing circuit to remove external noises and ripples superimposed on the battery power input, an autonomous circuit to kill the power supply when an abnormal condition occurs in the radio section, a detection circuit to detect voltage drops in the power input, and other components. There is also a protection circuit for reversed polarity connection.

7-8-2. Principles of Operation

(1) Power switch

The PS module is designed so that it can be switched on and off by the handset power switch alone, or by the automobile ignition switch and the handset power switch together. In the former case the on/off signal from the handset power switch is received through the rear multi-pin connector. In the latter case the handset power switch cannot turn the power on unless th ignition

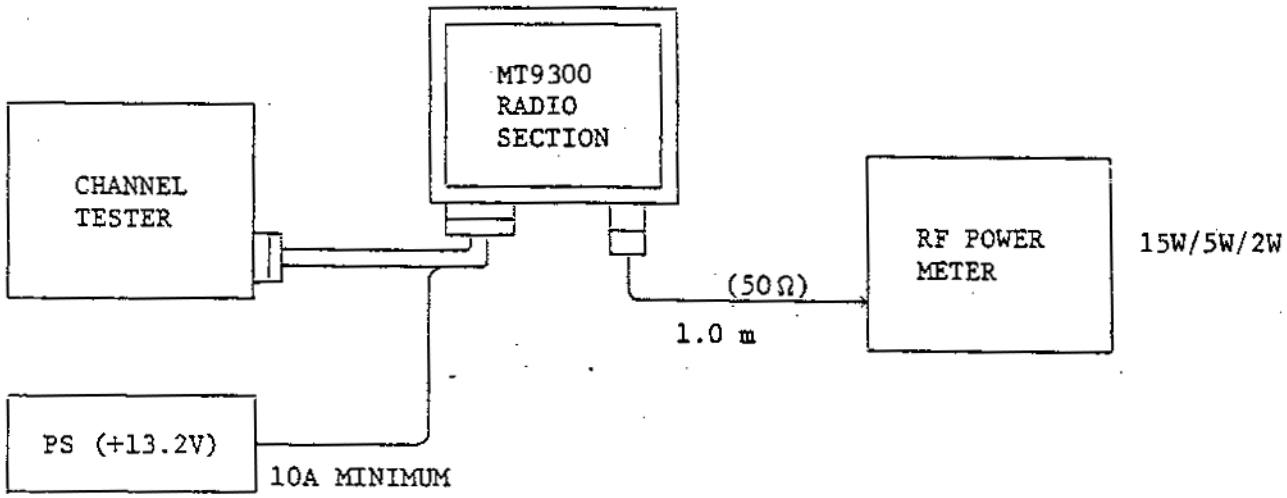

Figure 8-1 SETUP FOR MEASURING TRANSMITTER OUTPUT POWER

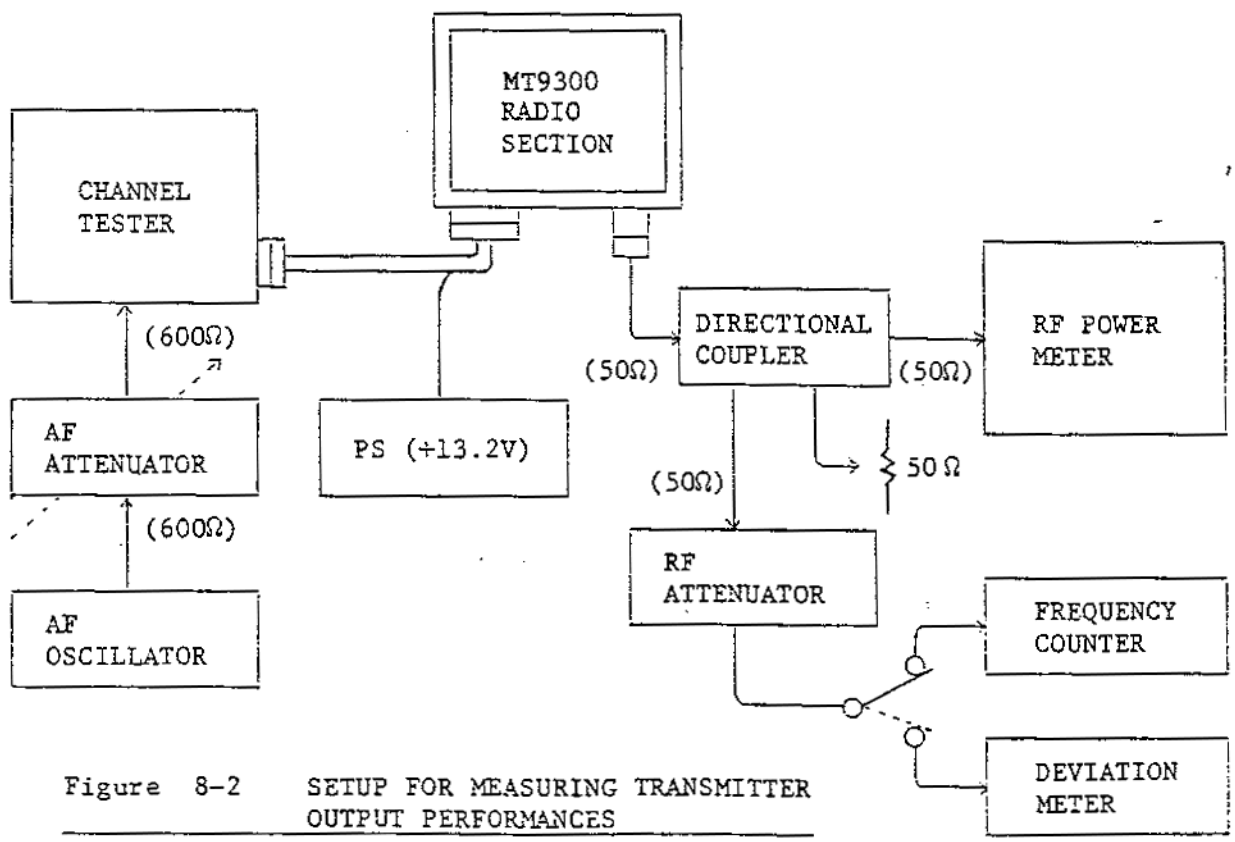

Figure 8-2 SETUP FOR MEASURING TRANSMITTER OUTPUT PERFORMANCES

switch is on beforehand.

The external battery is connected to the relay circuit of the PS module at pin 5 of connector Z207. When power is controlled by the handset power switch alone, Z207 pin 5 receives +13.2V power directly from the external battery. When power is controlled by the handset power and ignition switches together, the +13.2V power is routed to Z207 pin 5 through the ignition switch from the external battery.

The both handset power switch and ignition switch are not included in the radio section.

(2) Relay circuits

There are two relay circuits: the main relay circuit and the sub-relay circuit that drives the main relay. The +13.2V power input to Z207 pin 5 is passed through diode X2 to pin 3 of RL1 in the sub-relay circuit. The X2 diode acts as a reversed polarity connection protector; it prevents power from reaching the sub-relay circuit when the external battery is connected in the reverse polarity by mistake.

Pin 5 of RL1 is connected to the handset power switch through pin 6 of connector Z207 and drives this relay RL1 when the handset power switch on. When RL1 operates, pins 4 and 7 are connected at its contact r1 and pin 6 of the main relay RL2 and capacitor

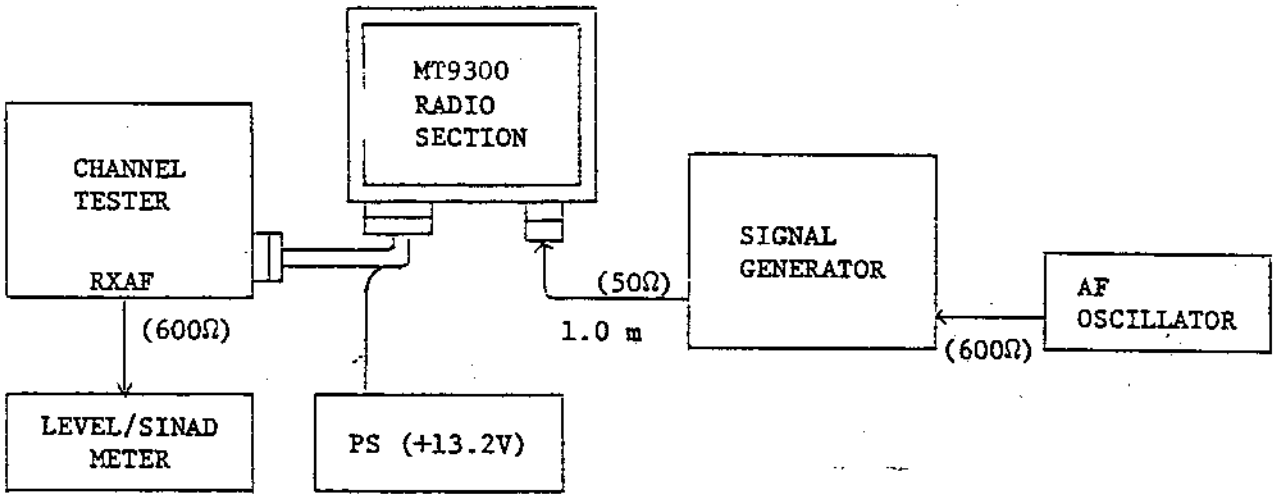

Figure 8-3 SETUP FOR MEASURING RECEIVER PERFORMANCES

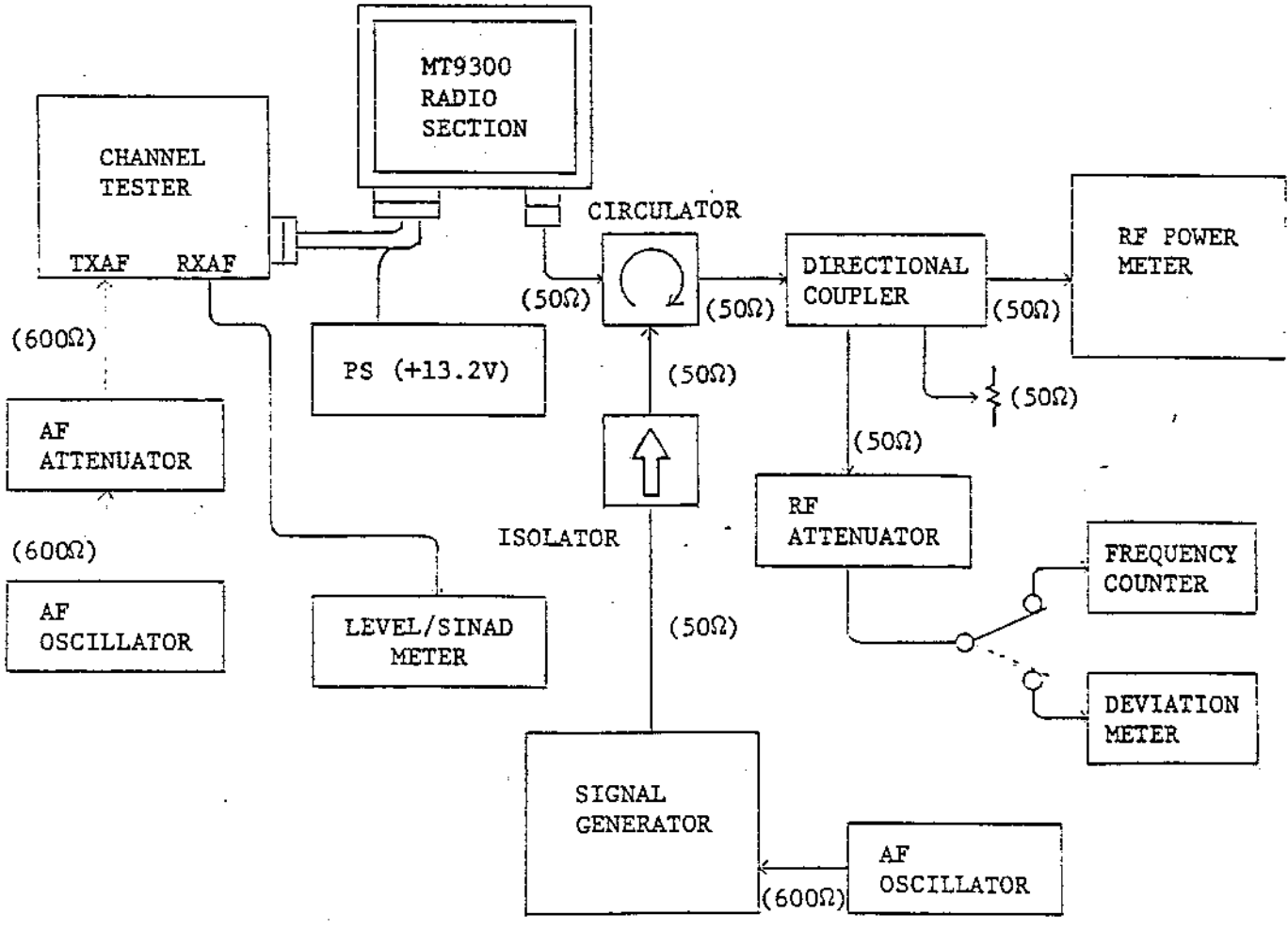

Figure 8-4 SETUP FOR COMPREHENSIVE MEASUREMENT

C6 are energized. The voltage from C6 turns on TR1 via R2 and X5, causing RL2 to operate. The +13.2V power supply supplied to pins 3 and 4 of connector Z207 from the external battery passes through pins 1 and 3 of RL2 which are connected at its contact r2 when RL2 operates, and the smoothing choke coil L1, then appears at pins 9 and 10 of connector Z207 as output. This output voltage is supplied to the handset, MCC, and all the modules of the radio section except the POW AMP module.

Because of the large current drain of the POW AMP module, its power is supplied directly from pin 3 of contact r2 of RL2 through a cord. When C6, the capacitor that turned TR1 on, is fully charged by the voltage applied across it through R2, it tries to turn TR1 off again, but the voltage output from L1 reaches TR1 through R3 and X6 to hold it in the on state and keep the circuit operating. The operation described above continues until the handset power switch or ignition switch is turned off.

(3) Smoothing circuit

The smoothing circuit is a low-pass filter consisting of L1, C4, and C5 that rejects ripple, spike, and other noises superimposed on the +13.2V input from the external battery.

(4) Autonomous circuit

The autonomous circuit turns the main relay off to stop power

supply when the following conditions continue for a few tens of seconds:

(a) The MCC operates abnormally.

(b) The transmitter is operated while there is no carrier input to the receiver.

The autonomous circuit consists of IC1, IC2, X8, TR2, and their peripheral circuits.

The autonomous clock signal (400 Hz: 2.5 ms) received from the MCC is directed to IC1 through pin 15 of connector Z207. IC1 is a fixed-frequency divider that divides the clock signal by 4,096 (2^{12}) and sends an output signal to TR2 at intervals of roughly 10 seconds. The output signal from TR2 turns off the main relay RL2 by acting through X6 to turn off TR1.

X8, C7, and R6 form a pulse generating circuit that resets the dividing count in IC1 at the start of operation, when power is turned on. The reset pulse is applied to pin 11 (the reset pin) of IC1 through a NAND gate, IC2 (4/4).

The autonomous reset signal from the MCC is fed to the NAND gate IC2 (2/4) through pin 13 of connector Z207. Since this autonomous reset signal is sent at intervals of less than 10 s, as long as the transceiver is operating normally, IC1 is reset before it reaches the top of its count.

The squelch detection signal (CDL) from the RX module is fed through pin 14 of connector Z207 to IC2 (1/4), which inverts it and sends it to IC2 (3/4). The power monitor signal from the POW AMP module is also brought to IC2 (3/4), via pin 12 of connector Z207. IC2 (3/4) is a NAND gate, and its output signal is directed via X7 to IC2 (2/4), which NANDs it with the autonomous reset signal, then supplies it to the reset pin of IC1 through another NAND gate in IC2 (4/4). When there coexists squelch detection signal and the power monitor signal, IC2 (2/4) prevents the autonomous reset signal from reaching IC1, allowing IC1 to count through one full cycle and turn the power supply off.

If the MCC malfunctions, it ceases output of the autonomous reset signal on its own, again allowing IC1 to count through one cycle and turn off the power supply.

(5) Input voltage drop detection circuit

If the input voltage from the battery remains continuously below +10.0V for about 30 seconds, and does not recover to normal within another approximately 10 seconds, the power supply is shut off by stopping the autonomous reset signal at IC2 (2/4). The voltage drop detection circuit consists of a Zener diode X10 that generates a reference voltage, and a pair of differential amplifiers, IC3 (1/2) and IC3 (2/2). Potentiometer RV1 is used to set the voltage drop detection threshold.